Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system comprising:

a logic design module operable to be used by one or more users to generate a logic design as part of an electrical circuit, wherein the logic design includes labels; and

a central database integrated with the logic design module and including a collection of modifiable values of signal parameters that are accessible by the logic design module, wherein the values of signal parameters are associated with the labels in the logic design;

wherein the logic design module is operable to

update the logic design to reflect modification of the values of the signal parameters in the central database by modifying the logic design to be compatible with the modified values of the signal parameters, and

to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The system of claim [[3]] 1 wherein the indicated design discrepancies include a bit width error.

5. (Previously Presented) The system of claim 1 wherein the signal parameters characterize a signal bit width.

6. (Previously Presented) The system of claim 1 wherein the signal parameters characterize a signal bit position.

7. (Currently Amended) A method comprising:

receiving an assignment of a value to a signal parameter;

maintaining the value of the signal parameter in a central database in association with an identifier of the signal parameter;

using the identifier of the signal parameter maintained in the central database to identify a first position in computer code for a logic design forming part of an electrical circuit;

modifying the computer code at the ~~second~~ first position to reflect the value;

using the identifier of the signal parameter maintained in the central database to identify a second position in the computer code for the logic design;

modifying the computer code at the ~~first~~ second position to reflect the value;

receiving an updated value of the signal parameter in the central database; ~~and~~

updating both the first position and the second position in the computer code for the logic design to reflect the updated value of the signal parameter; and

indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

8. (Canceled)

9. (Canceled)

10. (Currently Amended) The method of claim [[9]] 7 wherein automatically indicating design discrepancies occurring in the logic design includes graphically indicating a bit width error.

11. (Previously Presented) The method of claim 7 wherein the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width.

12. (Previously Presented) The method of claim 7 wherein the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position.

13. (Previously Presented) The method of claim 7 wherein the signal parameter characterizes a bit field and the value includes a value for the bit field.

14. (Canceled)

15. (Currently Amended) An apparatus comprising:

a central database accessible by one or more users, the central database including a collection of

identifiers of one or more bit width signal parameters and

values associated with each of the identifiers of the bit width signal parameters;

modification logic to allow a user to modify the values associated with the identifiers individually;

an interface to convey the identifiers and the associated values from the central database to a logic design module that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit.

Claims 16.-17. (Canceled)

18. (Currently Amended) A machine-accessible medium containing instructions which cause a machine to perform operations comprising:

receiving a value of a signal parameter that characterizes multiple bits of a multiple bit signal;

maintaining the value of the signal parameter in a central database;

using the value of the signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit that includes the multiple bit signal;

receiving an update to the value of the signal parameter in the central database; ~~and~~

updating the logic design with the updated value of the signal parameter by modifying the logic design to be compatible with the updated signal parameter; and

indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

19. (Canceled).

20. (Canceled)

21. (Currently Amended) The machine-accessible medium of claim [[20]] 18 wherein automatically indicating design discrepancies occurring in the logic design includes graphically indicating a bit width error.

22. (Previously Presented) The machine-accessible medium of claim 18 wherein the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width.

23. (Previously Presented) The machine-accessible medium of claim 18 wherein the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position.

24. (Canceled)

25. (Previously Presented) The machine-accessible medium of claim 18 further including instructions which cause a machine to perform operations comprising permitting one or more users to access the central database.

26. (Previously Presented) The method of claim 1, wherein the signal parameters define characteristics that characterize multiple bits of a multiple bit signal.

27. (Previously Presented) The method of claim 1, wherein the signal parameter defines a characteristic that characterizes multiple bits of a multiple bit signal.